

## MODERN ELECTRONIC TESTING: CHALLENGES AND DEVELOPMENTS

The historically unparalleled productivity improvement has been a driving force of the modern electronics industry. As device complexity grows and fabrication costs continue to fall, test is emerging as the largest expense in complex IC manufacturing. Test solutions have been unable to maintain the required 25-30% per year gain in productivity. In fact, the *cost of testing* a transistor in a complex IC is projected to approach the fabrication cost of the transistor within this decade - hardly a welcome fact for the integrated device manufacturers, foundries, fabless semiconductor companies and their test house partners etc. For some complex circuits test cost now approaches *half* of the total fabrication cost.

One key test cost driver is the emergence of new design and fabrication methodologies such as System-on-Chip (SOC). Since the last decade the System-on-Chip (SoC) integration has been rapidly evolving as a new IC manufacturing paradigm. It has been spurred by the recent advances in microelectronic technology leading to the availability of millions of gates in IC, incorporating multiple technologies (high-speed logic, DRAM, flash memory, analog blocks, etc.) in the circuit and thus allowing entire systems to be built on a single chip.

At the same time, ICs continue to exponentially increase in complexity and performance with their faster speeds, mixed signals and higher pin counts. Testing circuits of complex types has historically required diverse types of ATE (automated test equipment) and special methods. High-performance mixed-signal ATEs are now struggling to handle SoC devices that contain multiple circuit types (so, called IPs). This often leads to the need for multiple test insertions which is ultimately lengthening test times and raising manufacturing costs.

Test cost and time reduction have become an urgent economic imperative. Designers and IC manufacturers have finally realized that they can't simply jawbone test engineers and ATE companies into lowering the prices and increasing performance of the ever-more-complex systems that are required to test increasingly complex chips. More and more design engineers and IC companies are considering and implementing the Design-For-Test (DFT) and Built-In-Self-Test (BIST) approaches. By sacrificing some chip area and functionality, this dramatically reduces the test cost and time. The latest emerging development in the electronic test technology is the introduction of the flexible (modular) ATEs architecture where the test system can be specified and configured to address the need of the IC testing as early as at the time of the circuit design.

Another area of great importance and intensive research in semiconductor test technology (and in general in semiconductor manufacturing) is yield improvement. As half-pitch sizes shrink from micro- to nano-scale, the defect occurrence level is increasing. Thus defect detection and classification is fast becoming crucial diagnosis tools for systematic defects screening and maintaining high product quality and reliability. Defect detection serves to screen out faulty or unreliable devices while defect classification provides the necessary information on specific manufacturing problems that caused these defect. This knowledge can then lead to early prevention and pre-emption of process issues. Classification can also lead to yield prediction, accurate yield modelling, automated process control and fault diagnosis.

The semiconductor manufacturing industries currently employ rigorous data logging practices. Thus by taking advantage of the extensive data repositories which are now available, defect classification can be performed via data mining algorithms and artificial intelligence. This approach is faster and cheaper than failure analysis and can be incorporated into the test procedure without significantly increasing the cost of test.

The talk will provide an overview and describe some current challenges in electronic testing of integrated circuits and electronic systems. It will also present several new promising research results and engineering techniques leading to substantial increase in efficiency of testing of modern semiconductor devices at one of the world leading multinational semiconductor manufacturer.

## SPEAKERS



**SERGE DEMIDENKO** is Chair of Electrical and Computer Systems Engineering as well as Head of School of Engineering at Monash University Sunway campus, Malaysia.

During his career he progressed from an engineer to Head of Joint (Industry-Academy) Test Laboratory of a large electronic manufacturing company (around 12,000 staff) and Head of Department posts by working for academia and industry. Has been on the academic and research staff of institutions of higher learning of several countries including Belarus (Belarusian State University of Informatics and RadioElectronics), UK (Brunel, The University of West London), Italy (Politecnico di Milano), Singapore (Singapore Polytechnic) and New Zealand (Massey University, Palmerston North and Wellington campuses), etc.

Professor Serge Demidenko is a Fellow of IEEE and IET, and UK Chartered Engineer. He was a Vice-Chair of the Test Technology Technical Council (TTTC) for Asia & Pacific of the IEEE Computer Society (CS), Member of the IEEE CS Fellow Evaluation Committee and a Member of the TTTC Technical Meetings Review Committee, founder and first Chair of Malaysia IEEE I&M Chapter. Currently he is a Co-Chair of Technical Committee on Fault Tolerant Measurement (TC-32) of the IEEE I&M Society; founder and Chair of the Steering Committee of DELTA (IEEE International Symposium on Electronic Design, Test & Applications). He served as a Chair and Committee Member of numerous international conferences, symposia and workshops.

Professor Demidenko is an Associate Editor of six international journals including the *IEEE Transactions on Instrumentation and Measurement*, *Journal of Electronic Testing: Theory and Applications (JETTA)*, *International Journal of Intelligent Systems Technologies & Applications (IJISTA)*, etc.

Areas of research interests of Professor Demidenko include Electronic Design & Test, Fault-Tolerance, and Signal Generation & Processing. The list of his publications includes 4 books, more than 150 journal and conference papers. He is also a co-author of 25 engineering patents.



**MELANIE PO-LEEN OOI** is a Lecturer in Electrical and Computer Systems Engineering at Monash University Sunway campus, Malaysia.

She completed her MEngSc study at Monash University Malaysia in 2006, with co-supervision from Freescale Semiconductor (M). She is now at the final stage of her PhD study leading to new methodologies for defect detection and classification in semiconductor manufacturing. Through a close collaboration and joint research with Freescale Semiconductor (M), she has contributed to the development of new industrial methodologies for integrated circuit testing. At present she also closely collaborates with Texas Instruments (M).

Melanie Ooi is Secretary of IEEE Instrumentation & Measurement Malaysia Chapter and a technical consultant for the MSC Malaysia Multimedia Supercorridor Research & Development Grant Scheme.

Areas of her research interests include testing and design of microelectronic devices. She is an author of over 20 journal and conference papers.